LISTING OF CLAIMS

The listing of claims provided below replaces all prior versions, and listings, of claims in the application.

1. (Currently Amended) A switch, comprising:

a set of inputs;

a set of memory banks being equal in number to the set of inputs, each input capable of transferring a data stream into the set of memory banks, wherein the data stream of each input is to be distributed across each of the set of memory banks in accordance with a set of single bit control signals;

a rotating selector for generating the set of single bit control signals, wherein the rotating selector causes a different one of the set of single bit control signals to have a unique state in a given clock cycle; and

a set of outputs, the set of outputs being equal in number to the set of memory banks, each data stream that is distributed across each of the set of memory banks is to be output from at least one of the set of outputs.

2. (Original) A switch as recited in claim 1, wherein the data stream of each input is to be distributed across each of the set of memory banks such that each of the set of memory banks receives one or more differing portions of the data stream.

3. (Original) A switch as recited in claim 2, wherein the data stream that is distributed across each of the set of memory banks is to be output from at least one of the set of outputs by retrieving the one or more differing portions of the data stream and

transmitting the one or more differing portions of the data stream to the at least one of the set of outputs in a sequence that provides the data stream.

4. (Original) A switch as recited in claim 1, further comprising:

a first set of multiplexers, each of the first set of multiplexers connected to receive the set of inputs, each of the first set of multiplexers having a multiplexer output connected to one of the set of memory banks, each of the set of memory banks being connected to one of the first set of multiplexers, each of the first set of multiplexers connected to receive a selector signal for controlling which of the received set of inputs is to be transmitted to the multiplexer output in a given clock cycle.

5. (Currently Amended) A switch as recited in claim 4, wherein the selector signal to be received by each of the first set of multiplexers is defined by a particular sequence of the set of single bit control signals, a number of single bit control signals within the set of single bit control signals being equal in number to the set of inputs.

6. (Currently Amended) A switch as recited in claim 1 [[~~5~~]], ~~further comprising:~~

~~a rotating selector for generating the single bit signals sequenced to define the selector signal,~~ wherein the rotating selector causes ~~causing~~ one of the single bit control signals to have a first digital state and a remainder of the single bit control signals to have a second digital state in the given clock cycle, the rotating selector causing a different one of the single bit control signals to have the first digital state on successive clock cycles such that the first digital state rotates in a defined sequence among the single bit control signals on successive clock cycles.

7. (Original) A switch as recited in claim 4, wherein the first set of multiplexers and the selector signal received by each of the first set of multiplexers cause the data stream of each input to be distributed across each of the set of memory banks on successive clock cycles.

8. (Original) A switch as recited in claim 1, further comprising:

a second set of multiplexers, each of the second set of multiplexers connected to receive a multiplexer input from each of the set of memory banks, each of the second set of multiplexers having an output representing one of the set of outputs, each of the second set of multiplexers connected to receive a selector signal for controlling which received multiplexer input from each of the set of memory banks is to be transmitted to the output in a given clock cycle.

9. (Original) A switch as recited in claim 8, wherein the selector signal to be received by each of the second set of multiplexers is defined by a sequence of single bit signals being equal in number to the set of memory banks.

10. (Currently Amended) A switch as recited in claim 9, further comprising:

a second rotating selector for generating the single bit signals sequenced to define the selector signals for the second set of multiplexers ~~signal~~, the second rotating selector causing one of the single bit signals to have a first digital state and a remainder of the single bit signals to have a second digital state in the given clock cycle, the second rotating selector causing a different one of the single bit signals to have the first digital

state on successive clock cycles such that the first digital state rotates in a defined sequence among the single bit signals on successive clock cycles.

11. (Original) A switch as recited in claim 8, wherein the second set of multiplexers and the selector signal received by each of the second set of multiplexers cause the one or more differing portions of the data stream distributed across each of the set of memory banks to be retrieved and transmitted to the output on successive clock cycles such that the data stream is provided at the output.

12. (Currently Amended) A memory, comprising:

a number of inputs, each input capable of receiving a data stream to be stored in the memory;

a number of memory banks for storing data streams received by the number of inputs, the number of memory banks being equal to the number of inputs;

a first ratcheting distributor for distributing the data stream received by either of the number of inputs across the number of memory banks in accordance with a set of single bit control signals, wherein the first ratcheting distributor includes a first rotating selector for generating the set of single bit control signals such that a different one of the set of single bit control signals has a unique state in a given clock cycle ~~whereby one or more of the number of memory banks contains a distinct portion of the data stream~~;

a number of outputs, each output capable of providing the data stream previously stored in the memory; and

a second ratcheting distributor for providing the ~~distinct portion of the~~ data stream ~~contained within either of~~ distributed across the number of memory banks to either of the number of outputs.

13. (Currently Amended) A memory as recited in claim 12, wherein the first ratcheting distributor comprises:

a number of multiplexers, each of the number of multiplexers connected to receive the number of inputs, each of the number of multiplexers having an output connected to a different one of the number of memory banks, each of the number of multiplexers connected to receive a different selector signal defined by a particular sequence of the set of single bit control signals ~~in each cycle of a clock~~, the different selector signal being defined to control which of the number of inputs received by the multiplexer is to be transmitted to the output of the multiplexer for storage in one of the number of memory banks~~; and~~

~~a rotating selector for generating a number of single bit signals to be used to define the different selector signal received by each of the number of multiplexers~~.

14. (Currently Amended) A memory as recited in claim 13, wherein one of the number of single bit control signals has a first digital state and each of a remainder of the single bit control signals has a second digital state, ~~the rotating selector defined to generate the number of single bit signals in each cycle of the clock,~~ the rotating selector ~~further~~ defined to cause a different one of the number of single bit control signals to have the first digital state on successive cycles of the clock such that the first digital state rotates in a fixed sequence among the number of single bit control signals on successive cycles of the clock.

15. (Original) A memory as recited in claim 13, wherein the number of multiplexers and the different selector signal received by each of the number of

multiplexers in each cycle of the clock causes the data stream received by each of the number of inputs to be distributed across the number of memory banks.

16. (Currently Amended) A memory as recited in claim 12, wherein the second ratcheting distributor comprises:

a number of output multiplexers, each of the number of output multiplexers connected to receive an input from each of the number of memory banks, each of the number of output multiplexers having an output representing one of the number of outputs, each of the number of output multiplexers connected to receive a different selector signal in each cycle of a clock, the different selector signal being defined to control which input received from each of the number of memory banks is to be transmitted to the output in each cycle of the clock; and

a second rotating selector for generating a number of single bit signals to be used to define the different selector signal received by each of the number of output multiplexers.

17. (Currently Amended) A memory as recited in claim 16, wherein one of the number of single bit signals has a first digital state and each of a remainder of the single bit signals has a second digital state, the second rotating selector defined to generate the number of single bit signals in each cycle of the clock, the second rotating selector further defined to cause a different one of the number of single bit signals to have the first digital state on successive cycles of the clock such that the first digital state rotates in a fixed sequence among the number of single bit signals on successive cycles of the clock.

18. (Currently Amended) A memory as recited in claim 16, wherein the different selector signal received by one of the number of output multiplexers in each cycle of the clock causes a ~~each distinct~~ portion of the data stream contained within the number of memory banks to be provided to the output on successive clock cycles such that the data stream is provided to the output.

19. (Cancelled)

20. (Currently Amended) A method for operating a memory, comprising:

receiving a number of inputs, each of the number of inputs representing a data stream to be stored in the memory, each of the number of inputs being received simultaneously; ~~and~~

distributing the data stream associated with each of the number of inputs across a number of memory banks in accordance with a set of single bit control signals, wherein a portion of the data stream is stored in each of the number of memory banks as required to completely store the data stream; and

generating the set of single bit control signals such that a different one of the set of single bit control signals has a unique state in a given clock cycle, the unique state indicating which data stream is to have a portion of itself stored in a particular memory bank in the given clock cycle.

21. (Original) A method for operating a memory as recited in claim 20, further comprising:

using a ratcheting distributor to distribute the data stream associated with each of the number of inputs across the number of memory banks.

22. (Currently Amended) A method for operating a memory as recited in claim 21, wherein using the ratcheting distributor includes operating a number of multiplexers, each of the number of multiplexers being operated to receive the number of inputs, each of the number of multiplexers being further operated to receive a selector signal ~~for controlling~~ defined by a particular sequence of the set of single bit control signals, the selector signal used to control which of the number of inputs is transmitted to an output connected to one of the number of memory banks.

23. (Currently Amended) A method for operating a memory as recited in claim 22, wherein ~~using the ratcheting distributor further includes generating the selector signal received by each of the number of multiplexers,~~ the selector signal is ~~being~~ different for each of the number of multiplexers on each cycle of a clock, the selector signal for each of the number of multiplexers being repeated on a clock cycle count that is a multiple of the number of inputs.

24. (Original) A method for operating a memory as recited in claim 20, further comprising:

retrieving the portion of the data stream stored in each of the number of memory banks; and

transmitting the portion of the data stream stored in each of the number of memory banks to an output, the transmitting causing the data stream to be provided at the output.

25. (Original) A method for operating a memory as recited in claim 24, wherein the retrieving and the transmitting of the portion of the data stream stored in each of the number of memory banks is perform simultaneously for a number of data streams, each of the number of data streams being transmitted to different outputs.

26. (Original) A method for operating a memory as recited in claim 24, further comprising:

using a ratcheting distributor to retrieve and transmit the portion of the data stream stored in each of the number of memory banks.

27. (Original) A method for operating a memory as recited in claim 26, wherein using the ratcheting distributor includes operating a number of multiplexers, each of the number of multiplexers being operated to receive the portion of the data stream stored in each of the number of memory banks, each of the number of multiplexers being further operated to receive a selector signal for controlling which portion of the data stream stored in each of the number of memory banks is transmitted to the output.

28. (Original) A method for operating a memory as recited in claim 27, wherein using the ratcheting distributor further includes generating the selector signal received by each of the number of multiplexers, the selector signal being different for each of the number of multiplexers on each cycle of a clock, the selector signal for each of the number of multiplexers being repeated on a clock cycle count that is a multiple of the number of memory banks.